This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (Withdrawn) A wire for a display device transmitting a scanning signal or a data signal, the wire comprising:

a metal film including a conductive material; and

a metal oxide film formed on the metal film and including an oxide of a conductive material.

2. (Withdrawn) The wire of claim 1, wherein the wire includes a gate line or a data line of a liquid crystal display.

3. (Withdrawn) The wire of claim 1, wherein the metal film comprises one of Cr, Mo, Mo alloy, Al and Al alloy.

4. (Withdrawn) The wire of claim 1, wherein the metal oxide film comprises one of oxides of Cr, Mo and Mo alloy.

5. (Withdrawn) The wire of claim 1, wherein the conductive material included in the metal film and the conductive material included in the metal oxide film are substantially the same.

6. (Previously Presented) A thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and including a gate line and a gate electrode connected to the gate line;

a gate insulating film covering the gate wire;

a semiconductor layer formed on the gate insulating film;

a data wire formed on the gate insulating film or the semiconductor layer and including a data line, a source electrode connected to the data line and located on the semiconductor layer and a drain electrode formed on the semiconductor layer and located opposite the source electrode with respect to the gate electrode;

a passivation layer covering the data wire; and

a pixel electrode including a transparent conductive material or a reflective conductive material and connected to the drain electrode,

wherein the gate wire or the data wire comprises a metal film including a conductive material disposed on the insulating substrate or the gate insulating film and an opaque metal oxide film including an oxide of a conductive material disposed on the metal film,

wherein the opaque metal oxide film of the gate wire and the data wire block light, and a side of the metal film is uncovered by the opaque metal oxide film.

7. (Original) The thin film transistor array panel of claim 6, wherein the metal film comprises one of Cr, Mo, Mo alloy, Al and Al alloy.

8. (Previously Presented) The thin film transistor array panel of claim 6, wherein the opaque metal oxide film comprises one of oxides of Cr, Mo, Mo alloy, Al and Al alloy.

9. (Previously Presented) The thin film transistor array panel of claim 6, wherein the conductive material included in the metal film and the conductive material included in the opaque metal oxide film are substantially the same.

10. (Original) The thin film transistor array panel of claim 6, wherein the gate wire further includes a gate pad connected to the gate line, and the data wire further includes a data pad connected to the data line, and the thin film transistor array panel further comprises:

a subsidiary gate pad including substantially the same layer as the pixel electrode and connected to the gate pad; and

a subsidiary data pad including substantially the same layer as the pixel electrode connected to the data pads.

11. (Original) The thin film transistor array panel of claim 6, wherein the passivation film comprises SiOC, SiOF, SiNx or an organic insulating material.

12. (Original) The thin film transistor array panel of claim 6, wherein the semiconductor layer has substantially the same planar shape as the data wire excluding a channel portion between the source electrode and the drain electrode.

13. (Original) The thin film transistor array panel of claim 6, wherein the pixel electrode is located on the passivation layer, and the pixel electrode and the drain electrode are connected to each other via a first contact hole provided in the passivation layer.

14. (Withdrawn) A method of manufacturing a wire for a display device, the wire comprising: depositing a metal film on a substrate; depositing a metal oxide film on the metal film; and patterning the metal oxide film and the metal film under substantially the same etching condition to form a tapered structure.

15. (Withdrawn) The method of claim 14, wherein the metal film comprises Cr and the metal oxide film comprises CrOx.

16. (Withdrawn) The method of claim 15, wherein the etching condition includes wet etching using an etchant including 8-12% Ce(NH 4)2(NO3)6, 10-20% NH3 and remaining ultra pure water.

17. (Withdrawn) A method of manufacturing a thin film transistor array panel, comprising:

forming a gate wire on an insulating substrate, the gate wire including a gate line and a gate electrode connected to the gate line;

forming a gate insulating film covering the gate wire;

forming a semiconductor layer including amorphous silicon;

forming an ohmic contact layer including doped amorphous silicon on the semiconductor layer;

forming a data wire on the gate insulating film or the semiconductor layer, the data wire including a data line, a source electrode near the gate electrode, and a drain electrode located opposite the source electrode with respect to the gate electrode;

forming a passivation layer covering the semiconductor layer; and

forming a pixel electrode electrically connected to the drain electrode,

wherein the formation of the gate wire or the formation of the data wire comprises:

depositing a metal film;

depositing a metal oxide film; and

etching the metal oxide film and the metal film under substantially the same etching condition to make the gate wire or the data wire to have a tapered structure.

18. (Withdrawn) The method of claim 17, wherein the metal film comprises Cr and the metal oxide film comprises CrOx.

19. (Withdrawn) The method of claim 15, wherein the etching condition includes wet etching using an etchant including 8-12% Ce(NH 4)2(NO3)6, 10-20% NH3 and remaining ultra pure water.

20. (Previously Presented) The thin film transistor array panel of claim 6, wherein the opaque metal oxide film is formed on an entire top substantially horizontal surface of at least one of the data wire and the gate wire.

21. (Previously Presented) The thin film transistor array panel of claim 6, further comprising a plurality of color filters facing the pixel electrodes, wherein the plurality of color filters block light.

22. (Previously Presented) The thin film transistor array panel of claim 21, wherein portions of adjacent color filters of the plurality of color filters overlap with each other.

23. (Previously Presented) The thin film transistor array panel of claim 6, wherein the gate wire and the data wire transmits signals and block light leakage between pixel areas.

24. (Previously Presented) The thin film transistor array panel of claim 13, wherein the drain electrode comprises the metal film and the opaque metal oxide film, and the pixel electrode is connected to the metal film of the drain electrode.

25. (Previously Presented) The thin film transistor array panel of claim 6, wherein the side of the metal film includes opposing sidewalls defining the metal film and the sidewalls are uncovered by the opaque metal oxide film.